REMARKS

In the Office Action of March 19, 2004, claims 1 and 5-13 were rejected as being anticipated by or obvious over U.S. Patent 6,252,419 to Sung, et al. Claims 2-4 were indicated to be allowable.

As the Examiner appreciates, applicants' claim 1 is directed to signal routing apparatus comprising a register bank, a delay locked loop to generate a set of phase displaced signals, a phase controlled read circuit to sequentially route signals from the register bank in response to the phase displaced clock signals and an LVDS buffer connected to the read circuit to transmit the data signals in LVDS mode.

The Examiner has argued that Fig. 4 of the `419 patent discloses a register bank 48, a delay locked loop 16, a phase controlled read circuit 42 and an LVDS buffer 44. Further, the Examiner maintains that the delay locked loop generates a set of phase displaced clock signals citing Col. 7, lines 45-61.

The text at Col. 7, lines 45-61 refers to the phase lock loop circuit 617 shown in Fig. 2A of the `219 patent. This circuit is described as an alternative to PLL circuit 17 of Figs. 1 and 2 except that it has been modified to compensate for two delays at the same time. In particular, the circuit can provide for both local compensation at output 607 and global compensation at 604. However, the `419 patent does not indicate how circuit 617 might be used in the circuit of Fig. 4.

What Fig. 4 discloses is that one output of PLL circuit 16 is applied as unmultiplied clock output 246 to registers 48 to register data to outputs 49 of registers 48. The other output of PLL circuit is applied as a multiplied by W clock output 47 to shift register chain 42. Thus, register chain 42 does not receive a set of phase displaced clock signals but only receives one clock signal operating at a frequency that is W times the frequency of clock signal 246. But this is essentially the same situation depicted in the prior art circuit of Fig. 3 of the present application where the frequency of the clock signal used to drive each register bank 40 is seven times that of the standard clock signal. See page 2, lines 17-21.

As noted at page 3, line 11 of the present application, the present invention avoids the need to use higher rate clock signals and the disadvantages attendant thereto by applying a set of phase displaced clock signals to a phase controlled read circuit. One such set of phase developed clock signals is illustrated in Fig. 5 of the present application. As will be apparent, each edge of the clock signal is displaced by a distance T/8 (or 45°) from the corresponding edge of the adjacent clock signals in the set where T is the period of the clock signal. In contrast, in the circuit shown in Fig. 4 of the '419 patent, clock output 47 has a rate that is 8 x the clock rate of clock output 246 and clock output 47 is the only clock signal applied to read circuit 42. Since the

`419 patent does not disclose or suggest the application of a set of phase displaced clock signals to the read circuit and since it does not suggest the use of a phase controlled read circuit, it is respectfully submitted that claim 1 of the present application is patentable over the `419 patent.

Dependent claims 5-10 are patentable for the same reason claim 1 is patentable.

Independent method claim 11 recites the steps of generating a set of phase displaced signals and routing a set of data signals in response to the phase displaced signals. The '419 patent does not disclose the use of a set of phase displaced signals in routing a set of data signals.

Dependent claims 12 and 13 are patentable for the same reason claim 11 is patentable.

For the foregoing reasons, the claims presently pending in this application are believed to be patentable and this application is believed to be in condition for allowance.

No fees are believed due in connection with this response. However, the Commissioner is authorized to charge all required fees, fees under 37 C.F.R. § 1.17 and all required extension of time fees throughout the pendency of this application, or credit any overpayment, to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order No. 060889-0026-US).

Respectfully submitted,

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